PD - 94336c

International
IOR Rectifier

iP1001

iPOWIR™ TECHNOLOGY

Full Function Synchronous Buck Power Block

Integrated Power Semiconductors, Control IC & Passives

Features

- 3.3V to 12V input voltage①
- 20A maximum load capability, with no derating up to T_{PCB} = 90°C
- 5 bit DAC settable, 0.925V to 2V output voltage range ②
- Configurable down to 3.3Vin & up to 3.3Vout with simple external circuit ③
- 200kHz or 300kHz nominal switching frequency
- Optimized for very low power losses
- Over & undervoltage protection
- Adjustable lossless current limit
- Internal features minimize layout sensitivity *
- Very small outline 14mm x 14mm x 3mm

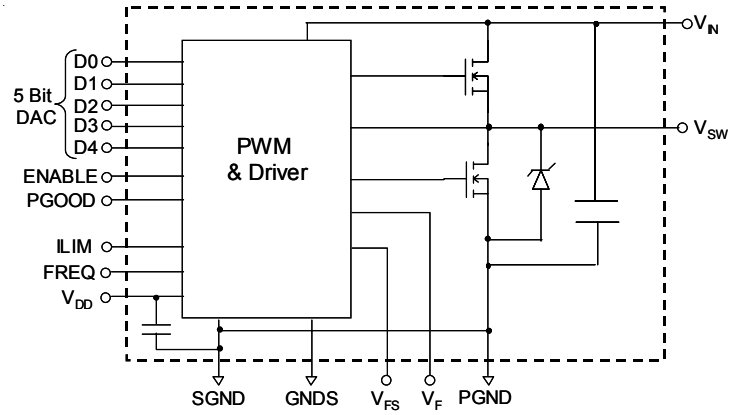
iP1001 Power Block

Description

The iP1001 is a fully optimized solution for high current synchronous buck applications requiring up to 20A. The iP1001 is optimized for single-phase applications, and includes a full function fast transient response PWM control, with an optimized power semiconductor chip-set and associated passives, achieving benchmark power density. Very few external components are required, including output inductor, input & output capacitors. Further range of operation to 3.3Vin can be achieved with the addition of a simple external boost circuit, and operation up to 3.3Vout can be achieved with a simple external voltage divider.

iPOWIR technology offers designers an innovative board space-saving solution for applications requiring high power densities. iPOWIR technology eases design for applications where component integration offers benefits in performance and functionality. iPOWIR technology solutions are also optimized internally for layout, heat transfer and component selection.

iP1001 Internal Block Diagram



* Although, all of the difficult PCB layout and bypassing issues have been addressed with the internal design of the iPOWIR block, proper layout techniques should be applied for the design of the power supply board. There are no concerns about unwanted shutdowns common to switching power supplies, if operated as specified. The iPOWIR block will function normally, but not optimally without any additional input decoupling capacitors. Input decoupling capacitors should be added at Vin pin for stable and reliable long term operation. No additional bypassing is required on the Vdd pin. See layout guidelines in datasheet for more detailed information.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units	Conditions
V_{IN} to PGND		-0.3	-	16.0	V	
V_{DD} to PGND		-0.3	-	6.0		
V_{FS}		-0.3	-	V_{DD}+0.3		
V_F		-0.3	-	V_{DD}+0.3		
D0-D4		-0.3	-	V_{DD}+0.3		
PGOOD to PGND		-0.3	-	6.0		
ENABLE to PGND		-0.3	-	6.0		
ILIM		-0.3	-	V_{DD}+0.3		
FREQ		-0.3	-	V_{DD}+0.3		
Output RMS Current		-	-	20	A	
Block Temperature	T_{BLK}	-40	-	125	°C	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Supply Voltage	V_{DD}	4.5	-	5.5	V	
Input Voltage Range ①	V_{IN}	3.3	-	12		With 4.5V<V_{DD}<5.5V
Output RMS Current from V_{SW} ④	$Iout_{VSW}$	-	-	20	A	
Output Voltage Range ②	V_{OUT}	0.925	-	2.0	V	DAC Setting see VID code, Table1.

Electrical Specifications @ V_{DD} = 5V & T_{PCB} 0°C - 90°C (Unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Power Loss	P_{LOSS}	-	3.1	3.9	W	300kHz, 12V_{IN}, 1.3Vout, 20A
Over Current Shutdown		-	25	-	A	V_{IN}=12V, V_{OUT}=1.3V, FREQ=300KHz, R_{LIM}=340k
Soft Start Time		-	1.8	-	ms	
Output Voltage Accuracy		-2	-	2	%	All DAC codes T_{BLK} = -40°C to 125°C
V_F Input Resistance		-	181	-	kΩ	
Frequency	FREQ	-	200	-	kHz	freq pin connected to V_{DD}
		-	300	-		freq pin floating
V_{DD} Undervoltage Lockout		-	4.2	-	V	200mV hysteresis
Output Undervoltage Shutdown Threshold		-	0.8	-	V	
Output Undervoltage Protection Blanking Time		-	20	-	ms	ENABLE going high on start-up
Output Overvoltage Shutdown Threshold at V_F		-	2.25	-	V	See OVP note in Design Guidelines
PGOOD Trip Threshold	PGOOD	-	V_{DAC} -5%	-	V	At V_F
PGOOD Leakage Current		-	1	-	µA	PGOOD output high Forced to 5.5V
PGOOD Output Low Voltage		-	-	0.4	V	I_{sink} = 1mA
Logic Input High Voltage		2.4	-	-	V	D0-D4, Enable
Logic Input Low Voltage		-	-	0.8	V	D0-D4, Enable

Electrical Specifications (continued)

Parameter	Symbol	Min	Typ	Max	Units	Conditions
V_{DD} Operating Current	I_{VDD}	-	25	-	mA	Enable High, 300kHz
V_{DD} Quiescent Current	I_{QVDD}	-	600	-	μA	Shutdown mode
V_{IN} Quiescent Current	I_{QVIN}	-	-	1	mA	Enable Low, VIN = 12V
ILIM to SGND Internal Resistance		-	300	-	kΩ	Measured ILIM pin to SGND

Notes :

① For Vin less than 4.5V requires external $5V_{DD}$ supply.

② Can be modified to operate up to $3.3V_{OUT}$, outside of DAC settable range. See Design Guidelines on how to set output voltage greater than 2V.

③ See design guidelines.

④ See Fig. 5 for Recommended Operating Area

Guaranteed Performance Curves

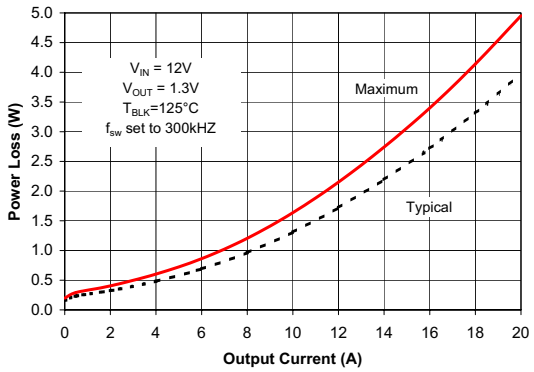


Fig 1. Power Loss vs Current

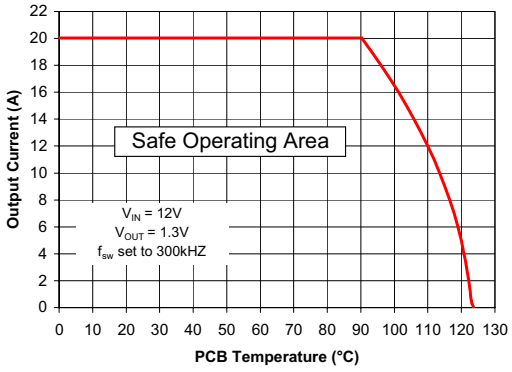


Fig 2. Safe Operating Area (SOA) vs T_{PCB}

Adjusting the Power Loss and SOA curves for different operating conditions

To make adjustments to the power loss curves in Fig. 1, multiply the normalized value obtained from the curves in Figs. 3, or 4 by the value indicated on the power loss curve in Fig. 1. If multiple adjustments are required, multiply all of the normalized values together, then multiply that product by the value indicated on the power loss curve in Fig. 1. The resulting product is the final power loss based on all factors.

To make adjustments to the SOA curve in Fig. 2, determine the maximum allowed PCB temperature in Fig. 2 at the required operating current. Then, add the correction temperature from the normalized curves in Figs. 3 or 4 to find the final maximum allowable PCB temperature. When multiple adjustments are required, add all of the temperatures together, then add the sum to the PCB temperature indicated on the SOA graph to determine the final maximum allowable PCB temperature based on all factors.

Note: If input voltage <5Vin nominal operation is required then first see Fig. 5 for maximum current capability limit.

Operating Conditions for the examples below:

Output Current = 20A Input Voltage = 7V
Output Voltage = 2.5V

Adjusting for Maximum Power Loss:

(Fig. 1) Maximum power loss =5 W
(Fig. 3) Normalized power loss for output voltage ≈1.14
(Fig. 4) Normalized power loss for input voltage ≈0.89

Adjusted Power Loss = 5W x 0.89 x 1.14 ≈ 5.07W

Adjusting for SOA Temperature:

(Fig. 2) SOA PCB Temperature = 90°C
(Fig. 3) Normalized SOA PCB Temperature for output voltage ≈ -4.5°C
(Fig. 4) Normalized SOA PCB Temperature for input voltage ≈ 4°C

Adjusted SOA PCB Temperature = 90°C + 4°C -4.5°C ≈ 89.5°C

Typical Performance Curves

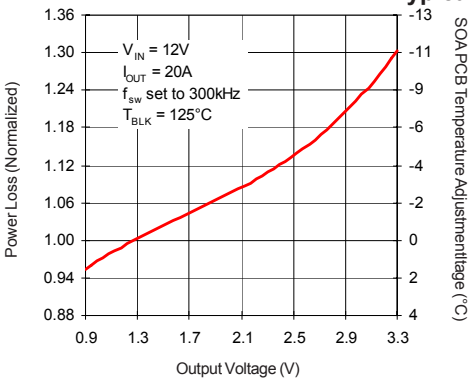


Fig 3. Normalized Power Loss vs V_{OUT}

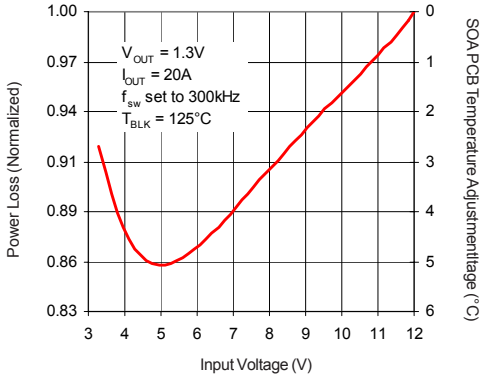


Fig 4. Normalized Power Loss vs V_{IN}

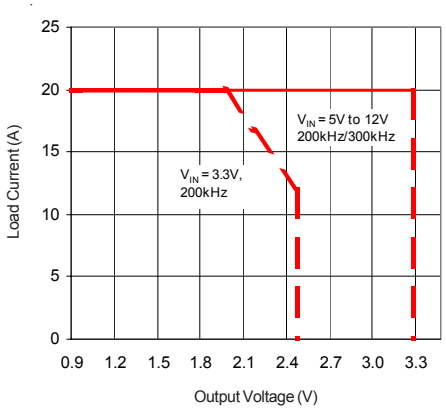


Fig 5. Recommended Operating Area

For 200kHz frequency setting there will be a 10% power loss reduction and a positive PCB temperature adjustment of 3°C.

D4	D3	D2	D1	D0	OUTPUT VOLTAGE(V)
0	0	0	0	0	2.00
0	0	0	0	1	1.95
0	0	0	1	0	1.90
0	0	0	1	1	1.85
0	0	1	0	0	1.80
0	0	1	0	1	1.75
0	0	1	1	0	1.70
0	0	1	1	1	1.65
0	1	0	0	0	1.60
0	1	0	0	1	1.55
0	1	0	1	0	1.50
0	1	0	1	1	1.45
0	1	1	0	0	1.40
0	1	1	0	1	1.35
0	1	1	1	0	1.30
0	1	1	1	1	Shutdown*
1	0	0	0	0	1.275
1	0	0	0	1	1.250
1	0	0	1	0	1.225
1	0	0	1	1	1.200
1	0	1	0	0	1.175
1	0	1	0	1	1.150
1	0	1	1	0	1.125
1	0	1	1	1	1.100
1	1	0	0	0	1.075
1	1	0	0	1	1.050
1	1	0	1	0	1.025
1	1	0	1	1	1.000
1	1	1	0	0	0.975
1	1	1	0	1	0.950
1	1	1	1	0	0.925
1	1	1	1	1	Shutdown*

* Shutdown : Upon receipt of the shutdown code (per VID code table above), both FETs are turned OFF and the output is discharged as the undervoltage protection is activated.

Table 1. VID Code Table②

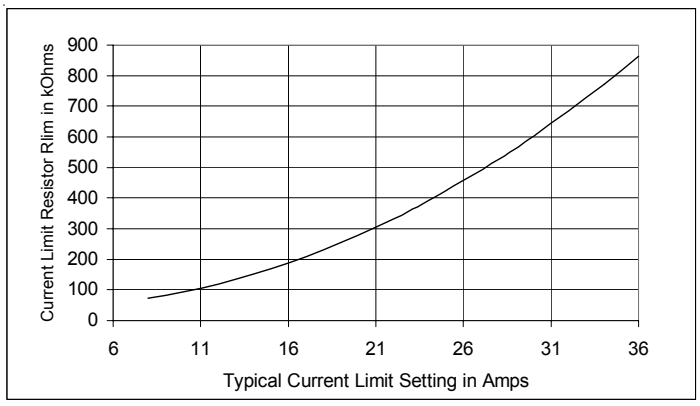


Fig 6. Overcurrent adjustment settings using R_{LIM}

Pin Name	Ball Designator	Pin Description
V_{IN}	A9-A12, B9-B12, C9-C14, D9-D14, E9-E16, F9-F16, G9-G16	Input voltage connection node.
NC	A1, A6-A7, A13-A15, B1, B6-B7, B13-B16, C3, C6-C7, C15-C16, D3-D4, D6, D15-D16 E3-E6, F1-F5, G1-G5, H1-H5, J1-J2, J6-J8, K6-K8, L6-L8, M6-M8, N4-N5, N7-N8, P4-P5, P7-P8, R6-R8, S6-S8	No electrical connection.
V_{SW}	H9-H14, J11-J14, K11-K14, L11-L14, N11-N14, M11-M14, P11-P14, R11-R14, S11-S14	Output inductor connection node.
PGND	H15-H16, J15-J16, K9-K10, K15-K16, L9-L10, L15-L16, M9-M10, M15-M16, N9-N10, N15-N16, P9-P10, P15-P16, R9-R10, R15-R16, S9-S10, S15-S16	Power ground.
V_{DD}	R4-R5, S4-S5	Control Power connection node
SGND	A2-A3, B2-B3	Signal ground.
GNDS	E1	Remote Ground Sense Pin. Connect to PGND for V_{OUT} >2V
ENABLE	R3, S3	Commands output ON or OFF. Active floating (internally pulled high). When logic low, the synchronous MOSFET is turned ON.
NC	R2, S2	No electrical connection, internally pulled high, must leave floating.
PGOOD	R1, S1	Internally pulled-up to V_{DD}.
V_F	C1-C2	Output voltage feedback local sense.
V_{FS}	D1-D2	Output voltage remote sense feedback signal. For greater than $2V_{OUT}$, disconnect from remote load and connect to V_F.
D0	P1-P2	VID code setting D/A inputs. Internally pulled high.
D1	N1-N2	
D2	M1-M2	
D3	L1-L2	
D4	K1-K2	
ILIM	A5, B5, C5	Current limit threshold setting pin. See ILIM curve for external resistor values.
FREQ	A4, B4	Switching frequency selector pin. Floating selects 300kHz, tied to V_{DD} selects 200kHz.

Table 2. Pin Description

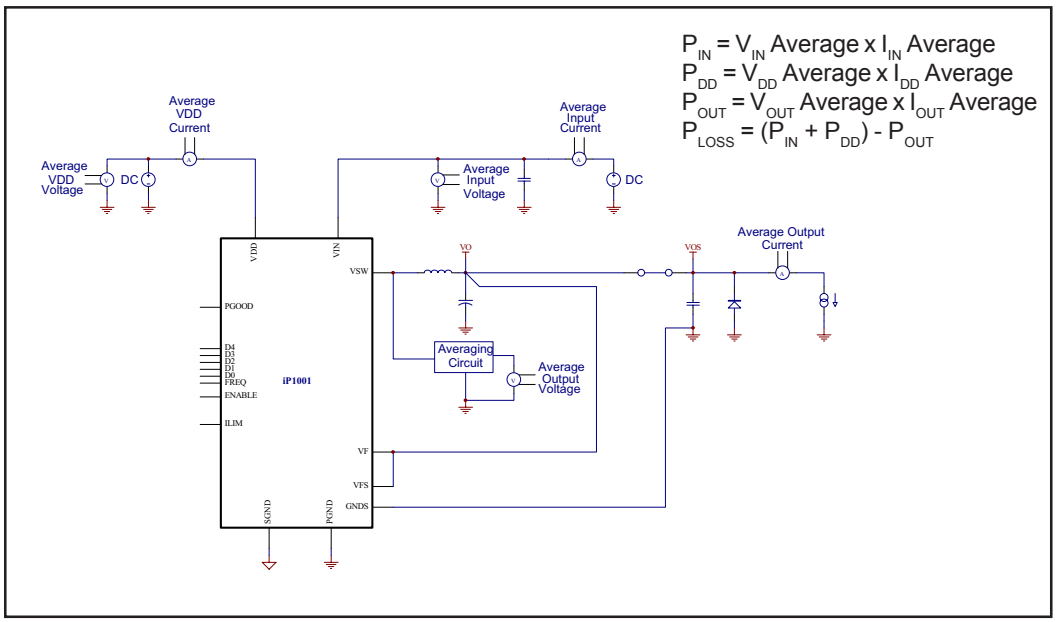


Fig 7. Power loss test circuit

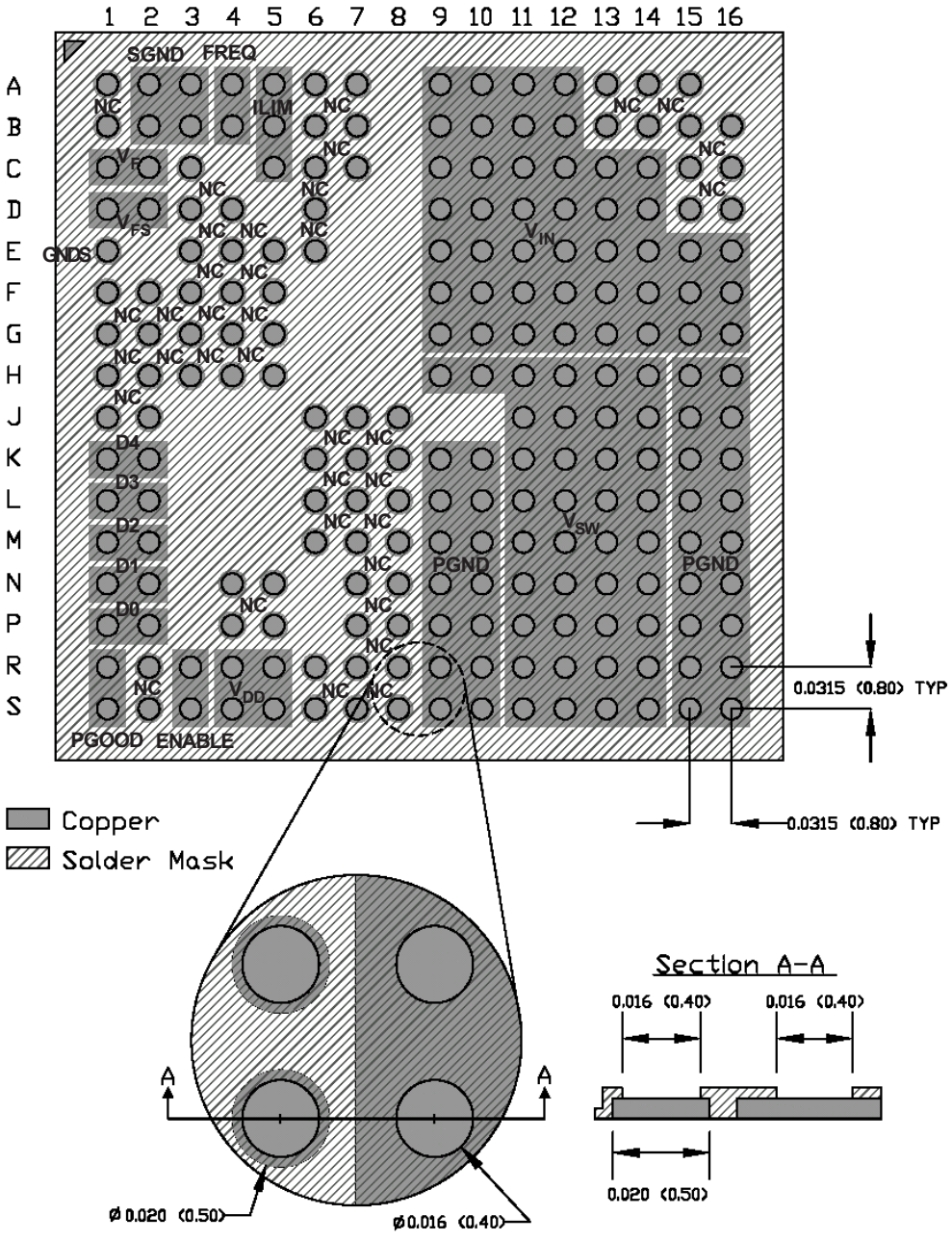


Fig 8. Recommended PCB Footprint (Top View)

iP1001 User's Design Guidelines

The iP1001 is a 20A power block that consists of optimized power semiconductors, PWM control and its associated passive components. It is based on a synchronous buck topology and offers an optimized solution where space, efficiency and noise caused by stray parasitics are of concern. The iP1001 components are integrated in a ball grid array (BGA) package where the electrical and thermal conduction is accomplished through solder balls.

FUNCTIONAL DESCRIPTION

V_{IN}

The standard iP1001 operating input voltage range is 5V to 12V. The input voltage can also be easily configured to run at voltages down to 3.3V.

FREQ

The PWM control is pseudo current mode. The ESR of the output filter capacitor is used for current sensing and the output voltage ripple developed across the ESR provides the PWM ramp signal.

iP1001 offers two switching frequency settings, 200kHz and 300kHz. At a given setting the switching frequency will remain relatively constant independent of load current.

V_{DD} (+5V bias)

An external 5V bias supply is required to operate the iP1001. In applications where input voltages are lower than 4.5V, and where 5V is not available, a special boost circuit is required to supply V_{DD} with 5V (as shown in the reference design).

Soft Start, V_{DD} Undervoltage Lockout

When V_{DD} rises above 4.2V a soft start is initiated by ramping the maximum allowable current limit. The ramp time is typically 1.8ms. An external capacitor can be added across the current limit resistor from ILIM to PGND to provide up to 5ms ramp time. Select the capacitor according to the 10nf/ms rule.

PGOOD

The PGOOD comparator constantly monitors V_F for undervoltage. A 5% drop in output voltage can cause PGOOD to go low. PGOOD pin is internally pulled-up to V_{DD} through a 100K, 5% resistor. If it is desired to use the PGOOD signal to enable another stage using iP1001, then it is recommended to filter and buffer PGOOD to prevent transients appearing at the output from pulling PGOOD low.

OVP (Output Overvoltage Protection)

If the overvoltage trip 2.25V threshold is reached, the OVP is triggered, the circuit is shutdown and the bottom FET is latched on discharging the output filter capacitor. Pulling ENABLE low resets the latch. The overvoltage trip threshold is scaled accordingly, if output voltages greater than 2V are set through voltage dividers.

UVP (Output Undervoltage Protection)

The Output Undervoltage Protection trip threshold is fixed at 0.8V. If ENABLE is pulled up and V_F is below 0.8V for a duration of 10-20ms, the PWM will be in a latched state, with the bottom FET latched on, and will not restart until ENABLE is recycled.

DAC Converter (D0-D4)

The output voltage is programmed through a 5-bit DAC (see the VID code in table 1). The output voltage can be programmed from 0.925V to 2V. To eliminate external resistors, the DAC pins are internally pulled up. To set for output voltages above 2V, the DAC must be set to 2V and a resistor divider, R3 & R4 (see Fig 10.), is used. The values of the resistors are selected using equation 1.

Equation 1 : $V_{out} = V_F \times (1 + R3/R4)$

where V_F is equal to the DAC setting

and R4 is recommended to be ~1kΩ

ENABLE	Bottom FET	Mode	Comments
Low	ON	Shutdown	
High	OFF	Shutdown	DAC code = X1111, Both FETs are turned OFF.
High	Switching	PWM (Running)	
High	ON	Fault	Fault latch set by OVP or UVP. This mode will sustain until V_{DD} is cycled or ENABLE is reset.

Table 3 - iP1001 Operating Truth Table

DESIGN PROCEDURE

Inductor Selection
The inductor is selected according to the following expression.

$$L = V_{OUT} \times (1-D) / (fsw \times \Delta I_L)$$

where, $D = V_{OUT} / V_{IN}$

V_{OUT} is the output voltage in Volts,
fsw is the switching frequency in kHz,
ΔI_L is the output inductor ripple current.

The inductor value should be selected from 0.8µH to 2.0µH range.

Output Capacitor Selection

Use tantalum or POSCAP type capacitors for iP1001. Selection of the output capacitors depends on several factors.

- Low effective ESR for ripple and load transient requirements.
- Stability.

To support the load transients and to stay within a specified voltage dip ΔV due to the transients, ESR selection should satisfy the following equation:

$$R_{ESR} \leq \Delta V/\Delta I$$

where, ΔI is the transient load step

If output voltage ripple is required to be maintained at specified levels then, the following expression should be used to select the output capacitors.

$$R_{ESR} \leq V_{p-p} / \Delta I_L$$

where, V_{p-p} is the peak to peak output voltage ripple.

The value of the output capacitor ESR zero frequency also determines stability. The value of the ESR zero frequency is calculated by the expression:

$$R_{ESR} = 1 / (2\pi \times f_{ESR} \times C_{OUT})$$

A 470µF POSCAP capacitor has a maximum 35mΩ of ESR which provides 9.7kHz zero frequency. The ESR zero frequency must be set below 12kHz. This value is calculated assuming the capacitor datasheet maximum ESR value.

Example:
To determine the amount of capacitance to meet a 30mVp-p output ripple, with 4A inductor current ripple requirement.

The calculated ESR will be = 30mV/4A = 7.5mΩ. This will require 5 x 470uF POSCAP capacitors. The total ESR will result in a 9.7kHz zero frequency.

For stable operation:

- **Set the resonant frequency f_o of the output inductor and capacitor between 2kHz and 4kHz.** The resonant frequency is calculated using the following expression:

$$f_o = 1/ (2\pi \times (\sqrt{LC}))$$

- **Select the output inductor value between 0.8µH to 2.0µH and the output capacitance between 1880µF (4x 470µF) and 5600µF (12x470µF)**

- **Set the minimum output ripple voltage to be greater than 0.5% of the output voltage.** Select the capacitor by ESR and by voltage rating rather than capacitance.

External Input Capacitor Selection

The switching currents impose RMS current requirements on the input capacitors. The following expression allows the selection of the input capacitors, based on the input RMS current:

$$I_{RMS} = I_{LOAD} \times (\sqrt{D} \times (1-D))$$

where, $D = V_{OUT}/V_{IN}$

Application Issues

Setting V_{OUT} above 2V

In certain applications where the output voltage is required to be set higher than the maximum DAC code setting of 2V, it is possible to use an external resistive voltage divider which, for accuracy, needs to have 1% or better tolerance. The switching frequency should be set at 200kHz by connecting the FREQ pin to V_{DD}. Also, the output voltage should never be set higher than 3.3V with a V_{IN} minimum of 5V, or 2.5V with a V_{IN} minimum of 3.3V. The DAC code should be set to 2V and the following equation used to select the resistors:

$$V_{OUT} = V_F \times (1 + R3/R4)$$

See the reference design for reference designators.

Note that the impedance at V_F is 180KΩ ±35%. It is recommended that R3 be calculated assuming a value of 1kΩ for R4. Connect V_{FS} to V_F and GNDS to PGND.

Duty Cycle $D = V_{OUT} / V_{IN}$ >50%

For duty cycles >50% the switching frequency should be set at 200kHz. 300kHz switching frequency can be selected if the output is less than 2V and the duty cycle is <50%.

For duty cycles >50%, add external compensation ramp from the Vsw terminal of the iP1001 device as shown in the reference design through R9 resistor and C21 capacitor (Fig 10a.). For optimum performance maintain a RC time constant of approximately 5μs.

Layout Guidelines

For stable and noise free operation of the whole power system it is recommended that the designer uses to the following guidelines.

1. Follow the layout scheme presented in Fig.9. Make sure that the output inductor L1 is placed as close to the iP1001 as possible to prevent noise propagation that can be caused by switching of power at the switching node V_{SW}, to sensitive circuits.

2. Provide a mid-layer solid ground with connections to the top layer through vias. The two PGND pads of the iP1001 also need to be connected to the same ground plane through vias.

3. Do not connect SGND pins of the iP1001 to PGND.

4. To increase power supply noise immunity, place input and output capacitors close to one another, as shown in the layout diagram. This will provide short high current paths that are essential at the ground terminals.

5. Although there is a certain degree of V_{IN} bypassing inside the iP1001, the external input decoupling capacitors should be as close to the device as possible.

6. In situations where the load is located at an appreciable distance from the iP1001 block, it is recommended that at least one or two capacitors be placed close to the iP1001 to derive the V_F signal.

7. The V_F connection to the output capacitors should be as short as possible and should be routed as far away from noise generating traces as possible.

8. V_{FS} & GNDS pins need to be connected at the load for remote sensing. If remote sensing is not used connect V_{FS} to V_F and GNDS to PGND.

9. Refer to IR application note AN-1029 to determine what size vias and what copper weight and thickness to use when designing the PCB.

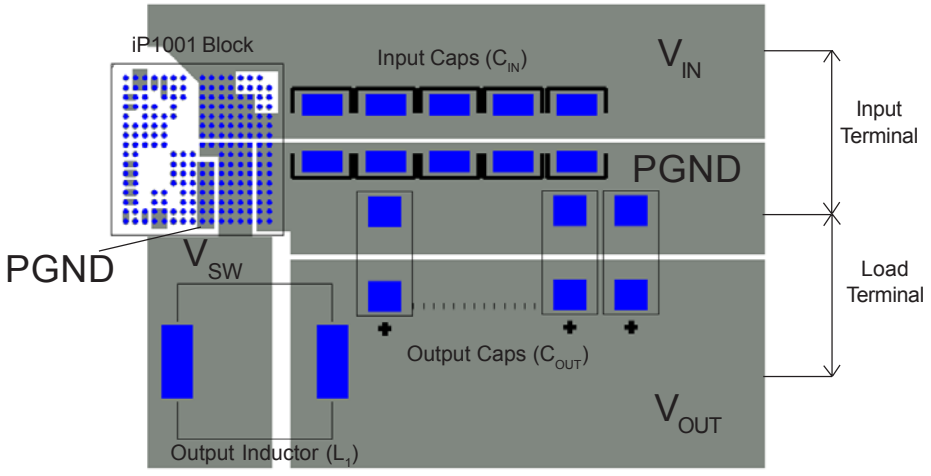


Fig 9. iP1001 suggested layout

iP1001 Reference Design

The schematics in Fig.10a & 10b and complete Bill of Materials in Table 4 are provided as a reference design to enable a preliminary evaluation of iP1001. They represent a simple method of applying the iP1001 solution in a synchronous buck topology. Fig. 10a shows the implementation for $<5V_{IN}$ nominal applications, and Fig. 10b shows the implementation for $5V_{IN}$ - $12V_{IN}$ nominal applications.

The connection pins are provided through the solder balls on the bottom layer of the package. A total power supply solution is presented with the addition of inductor L1 and the output capacitors C11-C14. Input capacitors C1-C10 are for bypassing in the $5V_{IN}$ - $12V_{IN}$ application, but only C1-C3 are required for $<5V_{IN}$ applications (refer to the BOM for values). Switches 1-5 of SW1 are used to program the output voltage. Refer to the VID table provided in this datasheet for the code that corresponds to the desired output voltage. Resistors R2 & R4 need to be removed for operation at standard VID levels (0.925V - 2.0V, leave R3 = 0Ω). Switch 8 of SW1 enables the output when floating (internally pulled high). The 5V V_{DD} power terminal and input power terminals are provided as separate inputs. They can be connected together if the application requires only 5V nominal input voltage.

The reference design also offers a higher output voltage option for greater than 2.0V, up to 3.3V. For output voltages above 2V, the DAC setting must be set to 2V, and then select resistors R3 & R4 per Equation 1 on page 10 for the desired output voltage. Remove R5 and connect V_F to V_{FS} through R2, where R2=0Ω. In this case, GNDS should be referenced to PGND. Tighter regulation can be achieved by using resistors with less than 1% tolerance. For Vin < 5V and Vout > 2V, the frequency select pin (FREQ) must be set to 200kHz (connected to V_{DD}).

For applications with V_{IN} < 5V and where there is no auxiliary 5V available, connections JP2 and JP3 must be provided in order to enable the boost circuit. This will provide 5V V_{DD} necessary for the iP1001 internal logic to function. The boost circuit will convert 3.3V input voltage to 5V, to power the V_{DD}, and will provide enough power to supply the internal logic for up to five iP1001 power blocks.

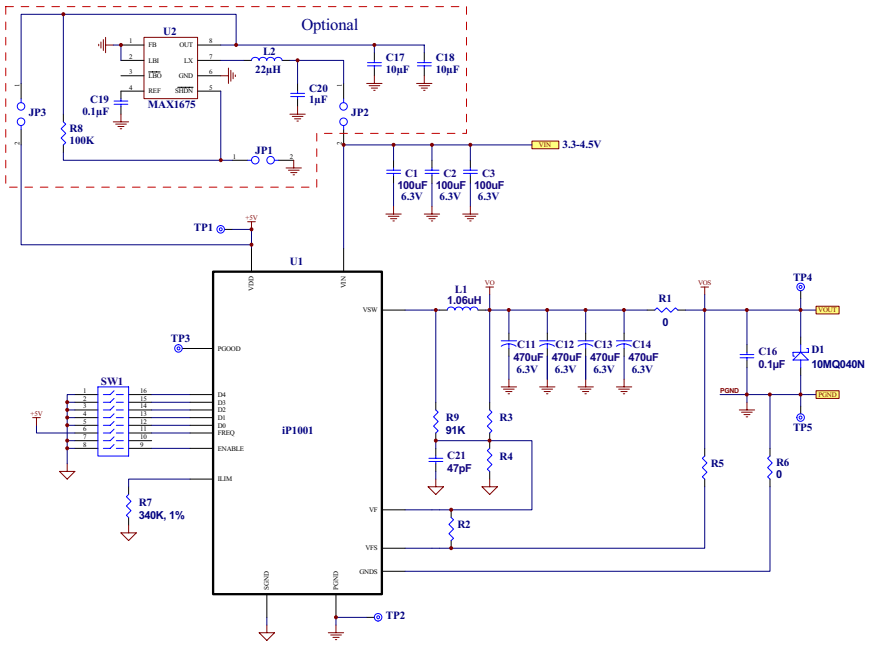


Fig 10a. - Reference Design Schematic For <4.5V$_{IN}$

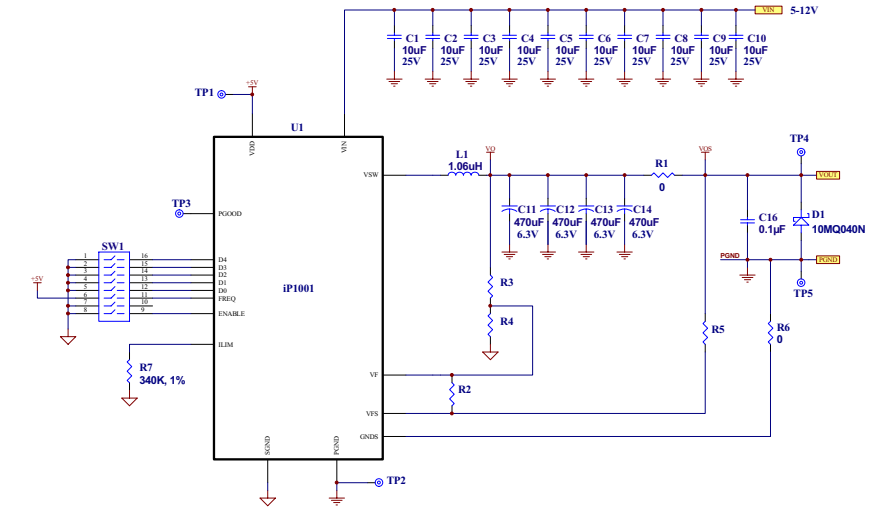


Fig 10b. - Reference Design Schematic For 5V$_{IN}$ - 12V$_{IN}$ Nominal

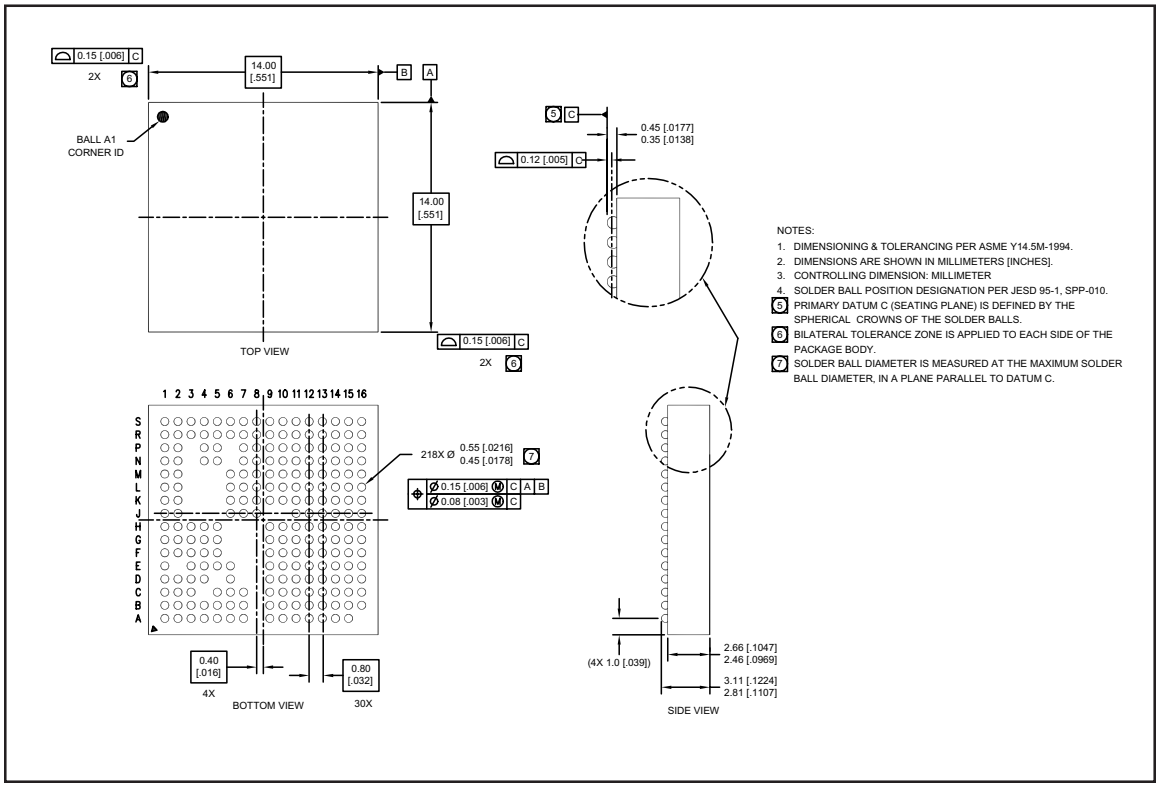
IRDCiP1001-A (For operation <4.5V_{IN})

Designator	Value	Part Type	Footprint	Mfr.	Mfr. P/N
C1, C3, C5	100uF	Capacitor, 6.3V, 20%, X5R	1812	TDK	C4532X5R0J107MT
C2, C4, C6, C7, C8, C9, C10, C15	-	Not Installed	-	-	-
C11, C12, C13, C14	470uF	Capacitor, 6.3V, 20%, Tantalum	7343	Sanyo	6TPB470M
C16, C19	0.100uF	Capacitor, 50V, 10%, X7R	1206	Novacap	1206B104K500N
C17, C18	10.0uF	Capacitor, 16V, 10%, X5R	1210	TDK	C3225X5R1C106KT
C20	1.00uF	Capacitor, 10V, 10%, X7R	0805	MuRata	GRM40X7R105K010
C21	47.0pF	Capacitor, 50V, 5%, C0G	1206	MuRata	GRM42-6C0G470J050A
D1	40V	Schottky Diode, 40V, 2.1A	D-64	International Rectifier	10MQ040N
JP1, JP2, JP3	-	Test Point	-	Samtec	TSW-102-07-LS
JP1-1, JP2-1, JP3-1	-	Shunt	-	Samtec	SNT-100-BKT
L1	1.06uH	Inductor, 16A, 20%, Ferrite	SMT	Panasonic	ETQP6F1R1BFA
L2	22uH	Inductor, 0.68A, 20%, Ferrite	SMT	Sumida	CR43-220
R1	0Ω	Resistor, 0Ω Jumper	2716	Isotek Corp	SMT-R000
R2	-	For <2Vout, Not installed For >2Vout, Resistor, 0Ω Jumper	SMT	-	-
R3	-	For <2Vout, Resistor, 0Ω Jumper For >2Vout see formula for value	SMT	-	-
R4	-	For <2Vout, Not installed For >2Vout recommend 1kΩ see formula for detail	SMT	-	-
R5	-	For <2Vout, Resistor, 0Ω Jumper For >2Vout, Not installed	1206	Panasonic	ERJ-8GEY0R00
R6	0Ω	Resistor, 0Ω Jumper	1206	-	-
R7	340kΩ	Resistor, 340kΩ, 1% 340kΩ sets for 20A limit. See ILIM formula for other values	1206	ROHM	MCR18EZHF3403
R8	100kΩ	Resistor, 100kΩ, 5%	1206	ROHM	MCR18EZHJ104
R9	91kΩ	Resistor, 91kΩ, 5%	1206	ROHM	MCR18EZHJ913
SW1	-	8-position DIP switch	SMT	C&K Components	SD08H0SK
TP1, TP3	-	Not Installed	-	-	-
TP2, TP4, TP5	-	Test Point	-	Keystone	1502-2
U1	-	Power Block	SSBGA 14mmx14mm	International Rectifier	iP1001
U2	-	IC, Step-Up DC-DC Converter, 0.5A	8uMAX	Maxim	MAX1675EUA

IRDCiP1001-B (For operation 5V_{IN} to 12V_{IN})

Designator	Value	Part Type	Footprint	Mfr.	Mfr. P/N
C1 C2 C3 C4 C5 C6 C7 C8 C9 C10	10.0uF	Capacitor, 25V, 10%, X5R	1812	MuRata	GRM43-2X5R106K25A
C11 C12 C13 C14	470uF	Capacitor, 6.3V, 20%, Tantalum	7343	Sanyo	6TPB470M
C16	0.100uF	Capacitor, 50V, 10%, X7R	1206	Novacap	1206B104K500N
C15, C17, C18, C19, C20, C21	-	Not Installed	-	-	-
D1	40V	Schottky Diode, 40V, 2.1A	D-64	International Rectifier	10MQ040N
JP1, JP2, JP3	-	Not Installed	-	-	-
JP1-1, JP2-1, JP3-1	-	Not Installed	-	-	-
L1	1.06uH	Inductor, 16A, 20%, Ferrite	SMT	Panasonic	ETQP6F1R1BFA
L2	-	Not Installed	-	-	-
R1	0Ω	Resistor, 0Ω Jumper	2716	Isotek Corp	SMT-R000
R2	-	For <2Vout, Not installed For >2Vout, Resistor, 0Ω Jumper	SMT	-	-
R3	-	For <2Vout, Resistor, 0Ω Jumper For >2Vout see formula for value	SMT	-	-
R4	-	For <2Vout, Not installed For >2Vout recommend 1kΩ see formula for detail	SMT	-	-
R5	-	For <2Vout, Resistor, 0Ω Jumper For >2Vout, Not installed	1206	Panasonic	ERJ-8GEY0R00
R6	0Ω	Resistor, 0Ω Jumper	1206	-	-
R7	340kΩ	Resistor, 340kΩ, 1% 340kΩ sets for 20A limit. See ILIM formula for other values	1206	ROHM	MCR18EZHF3403
R8, R9	-	Not Installed	-	-	-
SW1	-	8-position DIP switch	SMT	C&K Components	SD08H0SK
TP1 TP2 TP4 TP5	-	Test Point	-	Keystone	1502-2
TP3	-	Not Installed	-	-	-
U1	-	Power Block	SSBGA 14mmx14mm	International Rectifier	iP1001
U2	-	Not Installed	-	-	-

Table 4 - Reference Design Bill of Materials



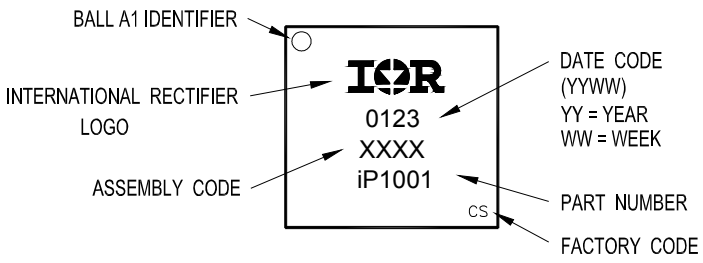
Mechanical Drawing

Refer to the following application notes for detailed guidelines and suggestions when implementing iPOWIR Technology products:

AN-1028: Recommended Design, Integration and Rework Guidelines for International Rectifier's iPOWIR Technology BGA Packages
This paper discusses the assembly considerations that need to be taken when mounting iPOWIR BGA's on printed circuit boards. This includes soldering, pick and place, reflow, inspection, cleaning and reworking recommendations.

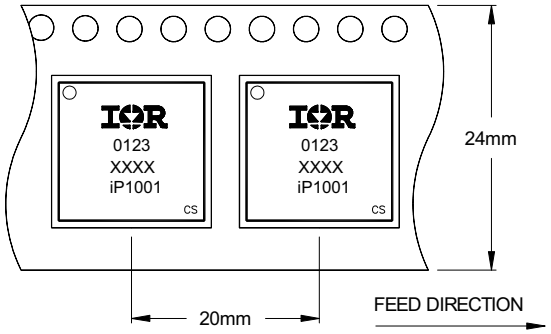
AN-1029: Optimizing a PCB Layout for an iPOWIR Technology Design
This paper describes how to optimize the PCB layout design for both thermal and electrical performance. This includes placement, routing, and via interconnect suggestions.

AN-1030: Applying iPOWIR Products in Your Thermal Environment
This paper explains how to use the Power Loss and SOA curves in the data sheet to validate if the operating conditions and thermal environment are within the Safe Operating Area of the iPOWIR product.

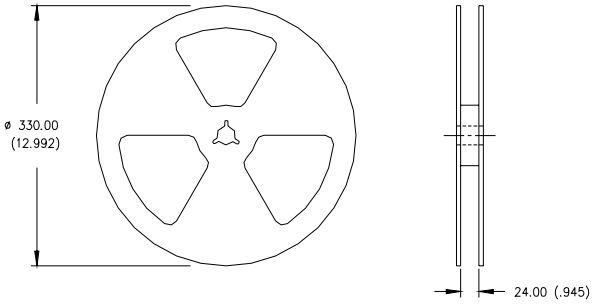


TOP

Part Marking



NOTES:
1. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Tape & Reel Information

Data and specifications subject to change without notice.
This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web site.

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